UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,398	03/24/2001	Khalid Sayood		7260

7590 02/05/2004

JAMES D. WELCH
10328 PINEHURST AVE.
OMAHA, NE 68124

EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	3

DATE MAILED: 02/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,398	SAYOOD ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover she t with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-16* is/are allowed.

6)☒ Claim(s) *1-11 and 17* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 18 is objected to because of the following informalities: On page 65, lines 11 and 16 of claim 18, "sysbol" is incorrect. It should be –symbol--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sayood et al. (Implementation issues in MAP joint source/channel coding, Proc. 22nd Annular Asilomar Conf. on Circuits, Systems, and Computers, pages 102-105, IEEE, November 1988) in view of Doshi et al. (US 6,349,138 B1) and Eerenstein et al. (US 5,097,151).

As per claim 1, Sayood et al. teach a variable length symbol (page 103, Sayood et al.), joint source-channel encoding (page 102, Sayood et al.), symbol decoding (page 104, Sayood et al.) and error correction system (page 102, Sayood et al.) comprising: encoder system (pages 102-103, Sayood et al.); modulation-transmission means i.e. a channel (page 102, Sayood et al.); and combination sequential, and encoded symbol, decoding systems (pages 102, 104, Sayood et al.);

Said encoder system comprising input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input there into (page 102, Sayood et al.);

Said encoder system being functionally interconnected to said modulation –transmission means such that entry of a symbol to said encoder system results in said encoder means outputting an encoded sequence of bits therefore into said modulation-transmission means (page 102, Sayood et al.).

The encoded symbol decoding system comprising means for initiating an error correction routine (page 102, Sayood et al.).

However Sayood et al. do not explicitly teach the specific use of the modulation-transmission means and combination sequential, and encoded symbol, decoding systems being functionally interconnected such that an encoded symbol sequence of bits entered to the modulation-transmission means enters the combination sequential, and encoded symbol, decoding systems. Sayood et al. also do not explicitly teach the specific use of a sequential decoding system. Sayood et al. do not explicitly teach the presence of an unexpected encoded reserved symbol, wherein the reserved symbol is not allowed as an input symbol to the symbol encoding system.

Doshi et al. in an analogous art teach that the output of the FEC encoder 215 is then prefixed with a framing byte at the framer 220, passed through a modulator 225 and broadcasted over the hybrid fiber/coax network 235 via a transmitter 230 for ultimate reception at individual cable modems 251 (figure 2, col. 7, lines 1-5, Doshi et al.). Doshi et al. teach that the payload is passed through the FEC decoder 255 (figure 2, col. 7, lines 12-13, Doshi et al.). Doshi et al. also teach that the exact number of decoders at the receiver may be one, as described herein with respect to sequential decoding or greater, if parallel decoding is desired (col. 17, lines 56-59, Doshi et al.). Doshi et al. teach that FEC is implemented by applying an algorithm to data to generate redundant bits at the transmitter (col. 1, lines 42-43, Doshi et al.). Doshi et al. also teach a forward error correction (FEC) encoder (item 215 in figure 2, col. 6, lines 61-62, Doshi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Doshi et al. by including an additional step of

using the modulation-transmission means and combination sequential, and encoded symbol, decoding systems being functionally interconnected such that an encoded symbol sequence of bits entered to the modulation-transmission means enters the combination sequential, and encoded symbol, decoding systems, using a sequential decoding system and the presence of an unexpected encoded reserved symbol, wherein the reserved symbol is not allowed as an input symbol to the symbol encoding system. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to transmit the encoded symbols to a receiver system with decoder in a separate location over the transmission system. The sequential decoding system and forward error correction is used at the receiver to detect and correct errors in the data received.

Sayood et al. also do not explicitly teach a system comprising a plurality of bistable elements and a selection from the group consisting of: at least one bistable element in the sequential decoding means is changed; and selection is made of a series of sequential bits, the selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in the sequential decoder means; is performed.

However Eerenstein et al. in an analogous art teach that the invention will be described in detail hereinafter with reference to the sequential finite-state machine whose state transition diagram is shown in FIG. 1. The FSM has 16 states and various transitions there between which are controlled by a clock signal and an input signal. The input signal is in this case a bivalent type ("0" or "1"). Generally speaking, an input signal may also consist of more bits. At instants, which are defined by the clock signal, for example at to each position going edge, the finite-state machine changes over to a next state. The state bearing the number 1 is absorbing in the case of a sequence of 5 successive input signals having the value "1": the rest state 1 is reached from any rest state after at the most 5 ones of the input signal. The given sequence of X values of the input signal [c(0), c(1), . . . , c(X-1)] in this case appears as follows: ["1", "1", "1", "1", "1"]; X=5 and N=4. It will be apparent that these values have been chosen merely by way of example; other choices are also possible. This sequential finite-state machine can be implemented in a circuit by means of 4 bistable element flip-flops (2 to the power of 4 implies 16 feasible

states), and a set of combinatory logic, which realizes the correct transitions between the states (figure 1, col. 3, lines 48-68, col. 4, lines 1-3, Eerenstein et al.).

Eerenstein et al. also teach that a sequential finite state machine circuit, comprising a set of N bistable elements [FF(1), . . . , FF(N)] and a set of combinatory logic connected thereto, the combination of logic values of the bistable elements defining a state of the circuit which is a representation of a state of a finite state machine, the circuit changing over to a next state at instants which are determined by a clock signal under the influence of the combinatory logic, the current state of the circuit, and an input signal, the set of combinatory logic realizing transitions between states of the finite-state machine in the circuit, characterized in that from any state a rest state is reached by way of a given sequence of X values of the input signal, [c(0), c(1), . . . , c(X-1)], starting with c(0) every sub-sequence [c(0), c(1), . . . , c(J-1)], having the length J, occurring in the given sequence of X values of the input signal, where 1<=J<=X, or a sub-sequence having the length J which is a one-to-one representation thereof being stored in the circuit.

The sequential finite-state machine circuit characterized in that the N bistable elements are presettable, the circuit being provided with (X-1) further bistable elements, coupled as a shift register, for the storage of the (X-1) most recent values of the input signal or values which are a one-to-one representation thereof, and is also provided with decoding logic, fed by the input signal and the (X-1) bistable elements of the shift register, which logic forms a detection signal as regards the occurrence of the given sequence of X values of the input signal, said detection signal being applied as a preset signal to the N presettable bistable elements (col. 7, lines 30-59, col. 8, lines 1-2, Eerenstein et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Eerenstein et al. by including an additional step of using a system comprising a plurality of bistable elements and upon the detecting of the presence of an unexpected encoded reserved symbol a selection from the group consisting of: at least one bistable element in the sequential decoding means is changed; and selection is made of a series of sequential bits, the selection being made from a group consisting of a plurality of such series of sequential bits which

result from the changing of bistable elements in the sequential decoder means; wherein the reserved symbol is not allowed as an input symbol to the symbol encoding system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to perform error correction by the decoder when an unexpected encoded symbol is received by the receiver.

- As per claim 2, Sayood et al., Doshi et al. and Eerenstein et al. teach the additional limitations.

Sayood et al. teach a variable length symbol (page 103, Sayood et al.) joint source-channel encoding (page 102, Sayood et al.), symbol decoding (page 104, Sayood et al.) and error correction system (page 102, Sayood et al.) comprising: encoder means (pages 102-103, Sayood et al.); modulation-transmission means i.e. a channel (page 102, Sayood et al.); and combination sequential, and encoded symbol, decoding means (pages 102, 104, Sayood et al.);

said encoder means comprising input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input there into (page 102, Sayood et al.);

said encoder means being functionally interconnected to said modulation-transmission means such that entry of a symbol to said encoder means results in said encoder means outputting an encoded sequence of bits therefore into said modulation-transmission means (page 102, Sayood et al.);

Doshi et al. teach the specific use of the encoder means further having means for generating, and in a sequence expected by said encoded symbol decoding means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said encoder means input means (FEC encoder 215 in figure 2, col. 1, lines 42-43, col. 6, lines 61-62, Doshi et al.).

Doshi et al. teach the modulation-transmission means and combination sequential, and encoded symbol, decoding means being functionally interconnected such that an encoded symbol sequence of bits entered to the modulation-transmission means enters the encoded symbol decoding means (figure 2, col. 7, lines 1-5, lines 12-13, Doshi et al.). Doshi et al. also teach a sequential decoding means (col. 17, lines 56-59,

Doshi et al.). Doshi et al. teach the encoded symbol decoding means comprising means for initiating an error correction routine to the end that, and the detecting of the presence of an unexpected encoded reserved symbol, or the absence of an expected encoded sequence of bits for a reserved symbol (FEC decoder 255 in figure 2, col. 2, lines 64-67, Doshi et al.).

Eerenstein et al. teach a system comprising a plurality of bistable elements; and a selection from the group consisting of: at least one bistable element in said sequential decoding means is changed; and selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in the sequential decoder means; is performed (figure 1, col. 3, lines 48-68, col. 4, lines 1-3, col. 7, lines 30-59, col. 8, lines 1-2, Eerenstein et al.).

- As per claim 3, Sayood et al., Doshi et al. and Eerenstein et al. teach the additional limitations.

Sayood et al. teach a joint source-channel encoding (page 102, Sayood et al.), symbol decoding (page 104, Sayood et al.) and error correction system (page 102, Sayood et al.) comprising: encoder means (pages 102-103, Sayood et al.); modulation-transmission means i.e. a channel (page 102, Sayood et al.); and decoding means (pages 102, 104, Sayood et al.);

wherein said encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input there into (page 102, Sayood et al.).

Doshi et al. teach that the decoding means comprises a functional combination of a sequential decoder means (col. 17, lines 56-59, Doshi et al.). Doshi et al. teach an encoded symbol decoder means (FEC decoder 255 in figure 2, col. 2, lines 64-67, Doshi et al.). Doshi et al. teach that the encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means; such that in use said encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof, said sequence of bits being caused to arrive at said decoding means (figure 2, col. 7, lines 1-5, lines 12-13, Doshi et al.). Doshi et al. teach that the encoded symbol decoder means having error detection means such that in use said encoded symbol decoder means, upon detecting the

presence of an unexpected encoded sequence of bits for reserved symbol, initiates an error correction routine, wherein said reserved symbol is not allowed as an input symbol to said symbol encoding means (FEC decoder 255 in figure 2, col. 2, lines 64-67, Doshi et al.).

Eerenstein et al. teach a system, which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and to the end that a selection from the group consisting of: at least one bistable element in said sequential decoding means is changed; and selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means; is performed (figure 1, col. 3, lines 48-68, col. 4, lines 1-3, col. 7, lines 30-59, col. 8, lines 1-2, Eerenstein et al.).

- As per claim 5, Sayood et al., Doshi et al. and Eerenstein et al. teach the additional limitations.

Sayood et al. teach a joint source-channel encoding (page 102, Sayood et al.), symbol decoding (page 104, Sayood et al.) and error correction system (page 102, Sayood et al.) comprising: encoder means (pages 102-103, Sayood et al.); modulation-transmission means i.e. a channel (page 102, Sayood et al.); and decoding means (pages 102, 104, Sayood et al.).

Sayood et al. teach that the encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input there into (page 102, Sayood et al.).

Doshi et al. teach that the decoding means comprises a functional combination of a sequential decoder means (col. 17, lines 56-59, Doshi et al.).

Doshi et al. teach that the encoder means further having means for generating and, in a sequence expected by said encoded symbol decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said encoder means input means (FEC encoder 215 in figure 2, col. 1, lines 42-43, col. 6, lines 61-62, Doshi et al.). Doshi et al. teach that the encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means; such that in use said encoder means receives a

sequence of allowed symbols at its input means and provides an encoded sequence of bits (figure 2, col. 7, lines 1-5, lines 12-13, Doshi et al.). Doshi et al. teach that the encoder means provides an encoded sequence of bits for at least some thereof in optional combination with a sequence of bits which represent at least one encoded reserved symbol in a pattern expected by said decoder means, said sequence of bits being caused to arrive at said decoding means (col. 1, lines 38-46, Doshi et al.); and said encoded symbol decoder means having error detection means such that in use said encoded symbol decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine (col. 2, lines 64-67, Doshi et al.).

Eerenstein et al. teach a system, which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits (figure 1, col. 3, lines 48-68, col. 4, lines 1-3, Eerenstein et al.). Eerenstein et al. teach a selection from the group consisting of: at least one bistable element in said sequential decoding means is changed; and selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means; is performed (figure 1, col. 7, lines 30-59, col. 8, lines 1-2, Eerenstein et al.).

5. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sayood et al. (Implementation issues in MAP joint source/channel coding, Proc. 22nd Annular Asilomar Conf. on Circuits, Systems, and Computers, pages 102-105, IEEE, November 1988), Doshi et al. (US 6,349,138 B1) and Eerenstein et al. (US 5,097,151) as applied to claims 3 and 5 above, and further in view of Kimura et al. (US 5,311,177).

As per claim 4, Sayood et al., Doshi et al. and Eerenstein et al. substantially teach the claimed invention described in claim 3 (as rejected above).

However Sayood et al., Doshi et al. and Eerenstein et al. do not explicitly teach specifically that the encoder means is an arithmetic encoder and the decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder.

Kimura et al. in an analogous art teach that FIG. 4 is a block diagram of the structure of a code transmitting apparatus in this embodiment. An arithmetic encoder 302 of a one-time 2-bits insertion system generates an arithmetic code 315. An arithmetic decoder 303 of a one-time 2-bits insertion system detects and processes the carry control signal by using the arithmetic code 315 supplied from the arithmetic encoder 302 (figure 4, col. 21, lines 17-19, lines 27-29, lines 40-43, Kimura et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Kimura et al. by including additionally that the encoder means is an arithmetic encoder and the decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using an arithmetic encoder and an arithmetic decoder would provide the opportunity to use data compressing/expanding method for high performance transmission with error detection.

- As per claim 6, Sayood et al., Doshi et al., Eerenstein et al. and Kimura et al. teach the additional limitations.

Kimura et al. teach that the encoder means is an arithmetic encoder and the decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder (figure 4, col. 21, lines 17-19, lines 27-29, lines 40-43, Kimura et al.).

6. Claims 7, 8, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sayood et al. (Implementation issues in MAP joint source/channel coding, Proc. 22nd Annular Asilomar Conf. on Circuits, Systems, and Computers, pages 102-105, IEEE, November 1988) in view of Doshi et al. (US 6,349,138 B1), Eerenstein et al. (US 5,097,151), Kimura et al. (US 5,311,177) and Tajima (JP 63215226 A).

As per claim 7, Sayood et al. teach a joint source-channel encoding (page 102, Sayood et al.), symbol decoding (page 104, Sayood et al.) and error correction system (page 102, Sayood et al.) comprising: an encoder system (pages 102-103, Sayood et al.); modulation-transmission means i.e. a channel (page 102, Sayood et al.); and decoding system (pages 102, 104, Sayood et al.); wherein the encoder system

comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input there into (page 102, Sayood et al.) and c. causing said encoder means to encode at least some of said plurality of symbols and output bits corresponding thereto into said modulation-transmission means (page 102, Sayood et al.).

However Sayood et al. do not explicitly teach specifically that the encoder system being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding system; such that in use the encoder system receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof, said sequence of bits being caused to arrive at said decoding system; and the decoder system having error detection means such that in use the decoder system, upon detecting the presence of an unexpected encoded reserved symbol, initiates an error correction routine; wherein said reserved symbol is not allowed as an input symbol to said symbol encoding system.

Doshi et al. in an analogous art teach that the output of the FEC encoder 215 is then prefixed with a framing byte at the framer 220, passed through a modulator 225 and broadcasted over the hybrid fiber/coax network 235 via a transmitter 230 for ultimate reception at individual cable modems 251 (figure 2, col. 7, lines 1-5, Doshi et al.). Doshi et al. teach that the payload is passed through the FEC decoder 255 (figure 2, col. 7, lines 12-13, Doshi et al.). Doshi et al. also teach that the exact number of decoders at the receiver may be one, as described herein with respect to sequential decoding or greater, if parallel decoding is desired (col. 17, lines 56-59, Doshi et al.). Doshi et al. teach that FEC is implemented by applying an algorithm to data to generate redundant bits at the transmitter (col. 1, lines 42-43, Doshi et al.). Doshi et al. also teach a forward error correction (FEC) encoder (item 215 in figure 2, col. 6, lines 61-62, Doshi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Doshi et al. by including an additional step of using the decoding system that comprises a functional combination of a sequential decoder system and the encoder system being functionally interconnected to the modulation-transmission means and the modulation-transmission means being functionally interconnected to the decoding system; such that in

use the encoder system receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof, said sequence of bits being caused to arrive at said decoding system; and the decoder system having error detection means such that in use the decoder system, upon detecting the presence of an unexpected encoded reserved symbol, initiates an error correction routine; wherein the reserved symbol is not allowed as an input symbol to said symbol encoding system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to transmit the encoded symbols to a receiver system with decoder in a separate location over the transmission system. The sequential decoding system and forward error correction is used at the receiver to detect and correct errors in the data received.

Sayood et al. also do not explicitly teach the specific use of the system that comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits and a selection from the group consisting of: at least one bistable element in said sequential decoding means is changed; and selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means; is performed.

However Eerenstein et al. in an analogous art teach that the invention will be described in detail hereinafter with reference to the sequential finite-state machine whose state transition diagram is shown in FIG. 1. The FSM has 16 states and various transitions there between which are controlled by a clock signal and an input signal. The input signal is in this case a bivalent type ("0" or "1"). Generally speaking, an input signal may also consist of more bits. At instants, which are defined by the clock signal, for example at to each position going edge, the finite-state machine changes over to a next state. The state bearing the number 1 is absorbing in the case of a sequence of 5 successive input signals having the value "1": the rest state 1 is reached from any rest state after at the most 5 ones of the input signal. The given sequence of X values of the input signal [c(0), c(1), . . . , c(X-1)] in this case appears as follows: ["1", "1", "1", "1", "1"]; X=5 and N=4. It will be apparent that these values have been chosen merely by

way of example; other choices are also possible. This sequential finite-state machine can be implemented in a circuit by means of 4 bistable element flip-flops (2 to the power of 4 implies 16 feasible states), and a set of combinatory logic, which realizes the correct transitions between the states (figure 1, col. 3, lines 48-68, col. 4, lines 1-3, Eerenstein et al.).

Eerenstein et al. also teach that a sequential finite state machine circuit, comprising a set of N bistable elements [FF(1), . . . , FF(N)] and a set of combinatory logic connected thereto, the combination of logic values of the bistable elements defining a state of the circuit which is a representation of a state of a finite state machine, the circuit changing over to a next state at instants which are determined by a clock signal under the influence of the combinatory logic, the current state of the circuit, and an input signal, the set of combinatory logic realizing transitions between states of the finite-state machine in the circuit, characterized in that from any state a rest state is reached by way of a given sequence of X values of the input signal, [c(0), c(1), . . . , c(X-1)], starting with c(0) every sub-sequence [c(0), c(1), . . . , c(J-1)], having the length J, occurring in the given sequence of X values of the input signal, where 1<=J<=X, or a sub-sequence having the length J which is a one-to-one representation thereof being stored in the circuit.

The sequential finite-state machine circuit characterized in that the N bistable elements are presettable, the circuit being provided with (X-1) further bistable elements, coupled as a shift register, for the storage of the (X-1) most recent values of the input signal or values which are a one-to-one representation thereof, and is also provided with decoding logic, fed by the input signal and the (X-1) bistable elements of the shift register, which logic forms a detection signal as regards the occurrence of the given sequence of X values of the input signal, said detection signal being applied as a preset signal to the N presettable bistable elements (col. 7, lines 30-59, col. 8, lines 1-2, Eerenstein et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Eerenstein et al. by including an additional step of using the system that comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits and a selection from the group consisting of: at least one bistable element in said sequential decoding means is changed; and selection is made of a series of sequential bits, said

selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means; is performed.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to perform error correction by the decoder when an unexpected encoded symbol is received by the receiver.

Sayood et al. also do not explicitly teach specifically that the encoder means is an arithmetic encoder and the decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder.

However Kimura et al. in an analogous art teach that FIG. 4 is a block diagram of the structure of a code transmitting apparatus in this embodiment. An arithmetic encoder 302 of a one-time 2-bits insertion system generates an arithmetic code 315. An arithmetic decoder 303 of a one-time 2-bits insertion system detects and processes the carry control signal by using the arithmetic code 315 supplied from the arithmetic encoder 302 (figure 4, col. 21, lines 17-19, lines 27-29, lines 40-43, Kimura et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Kimura et al. by including additionally that the encoder means is an arithmetic encoder and the decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using an arithmetic encoder and an arithmetic decoder would provide the opportunity to use data compressing/expanding method for high performance transmission with error detection.

Sayood et al. also do not explicitly teach specifically that the decoding system comprises a functional combination of a sequential decoder system and an arithmetic decoder system.

However Tajima in an analogous art teaches that to reduce the number of processing steps, and to improve the processing speed by constituting the titled (i.e. sequential) decoder of a syndrome forming device, a buffer memory inputting and preserving a syndrome series and preserving and outputting an error series, a sequential decoding arithmetic circuit, and a correcting circuit correcting a data

corresponding to an information symbol in a received data. A sequential decoding arithmetic circuit has a state trellis corresponding to the syndrome forming device in its inside to transit the state of trellis based on the syndrome series fetched from a buffer memory (abstract, Tajima).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Tajima by including additionally that the decoding system comprises a functional combination of a sequential decoder system and an arithmetic decoder system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding system comprising a functional combination of a sequential decoder system and an arithmetic decoder system would provide the opportunity to pass acceptable sequences of the signals and discard unacceptable sequences of the signals and to use data compressing/expanding method for high performance transmission with error detection.

- As per claim 8, Sayood et al., Doshi et al., Eerenstein et al., Kimura et al. and Tajima teach the additional limitations.

Sayood et al. teach a joint source-channel encoding (page 102, Sayood et al.), symbol decoding (page 104, Sayood et al.) and error correction system (page 102, Sayood et al.) comprising: an encoder means (pages 102-103, Sayood et al.); modulation-transmission means i.e. a channel (page 102, Sayood et al.); and decoding means (pages 102, 104, Sayood et al.).

Sayood et al. teach that the encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input there into (page 102, Sayood et al.).

Doshi et al. teach a sequential decoder means (col. 17, lines 56-59, Doshi et al.).

Doshi et al. teach the encoder means further having means for generating and, in a sequence expected by the decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol

to the encoder means input means (FEC encoder 215 in figure 2, col. 1, lines 42-43, col. 6, lines 61-62, Doshi et al.).

Doshi et al. teach that the encoder means is functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means (figure 2, col. 7, lines 1-5, lines 12-13, Doshi et al.).

Doshi et al. teach that the encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof in optional combination with at least one encoded reserved symbol in a pattern expected by the decoder means, said sequence of bits being caused to arrive at said decoding means (col. 1, lines 38-46, Doshi et al.); and the decoder means having error detection means such that in use the decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine; wherein said reserved symbol is not allowed as an input symbol to said symbol encoding system (col. 2, lines 64-67, Doshi et al.).

Eerenstein et al. teach a system, which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits (figure 1, col. 3, lines 48-68, col. 4, lines 1-3, Eerenstein et al.).

Eerenstein et al. teach a selection from the group consisting of: at least one bistable element in said sequential decoding means is changed; and selection is made of a series of sequential bits, the selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means; is performed (figure 1, col. 7, lines 30-59, col. 8, lines 1-2, Eerenstein et al.).

Kimura et al. teach that the encoder means is an arithmetic encoder and the decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder (figure 4, col. 21, lines 17-19, lines 27-29, lines 40-43, Kimura et al.).

Tajima teaches that the decoding means comprises a functional combination of a sequential decoder means and an arithmetic decoder means (abstract, Tajima).

- As per claim 10, Sayood et al., Doshi et al., Eerenstein et al., Kimura et al. and Tajima teach the additional limitations.

Claim 10 (method) follows the same limitations as claim 7 (system). See rejection to claim 7, above. Claim 10 is rejected under the same rational as to claim 7 rejected above.

- As per claim 11, Sayood et al., Doshi et al., Eerenstein et al., Kimura et al. and Tajima teach the additional limitations.

Claim 11 (method) follows the same limitations as claim 8 (system). See rejection to claim 8, above. Claim 11 is rejected under the same rational as to claim 8 rejected above.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sayood et al. (Implementation issues in MAP joint source/channel coding, Proc. 22nd Annular Asilomar Conf. on Circuits, Systems, and Computers, pages 102-105, IEEE, November 1988) in view of Doshi et al. (US 6,349,138 B1), Eerenstein et al. (US 5,097,151) and Agazzi (US 6,236,645 B1).

As per claim 9, Sayood et al. teach a method of correcting errors in decoded symbols which are encoded by an encoder means in a joint source-channel coding system (page 102, Sayood et al.), comprising the steps of:

a. providing a joint source-channel encoding (page 102, Sayood et al.), symbol decoding (page 104, Sayood et al.) and error correction system (page 102, Sayood et al.) comprising: encoder means (pages 102-103, Sayood et al.); modulation-transmission means i.e. a channel (page 102, Sayood et al.); and decoding means (pages 102, 104, Sayood et al.)

Sayood et al. teach that the encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input there into, b. inputting a plurality of symbols to the input means of said encoder means and c. causing the encoder means to encode at least some of the plurality of symbols and output bits corresponding thereto into the modulation-transmission means (page 102, Sayood et al.).

However Sayood et al. do not explicitly teach specifically the encoder means further having means for generating and, in a sequence expected by said encoded symbol decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said encoder means input means; the encoder means being functionally interconnected to said modulation-transmission means and said

modulation-transmission means being functionally interconnected to said decoding means; such that in use said encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof, in optional combination with at least one encoded reserved symbol in a pattern expected by said decoder means, said sequence of bits being caused to arrive at said decoding means; and said encoded symbol decoder means having error detection means such that in use said encoded symbol decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine and e. causing said encoded symbol decoder means to, if detecting a present unexpected or absent expected, encoded reserved symbol perform a selection from the group.

Doshi et al. in an analogous art teach that the output of the FEC encoder 215 is then prefixed with a framing byte at the framer 220, passed through a modulator 225 and broadcasted over the hybrid fiber/coax network 235 via a transmitter 230 for ultimate reception at individual cable modems 251 (figure 2, col. 7, lines 1-5, Doshi et al.). Doshi et al. that at the receiver, data is first FEC decoded and then descrambled. Therefore FEC is utilized at the receiver to identify and correct bit errors introduced during transmission (col. 2, lines 64-67, Doshi et al.). Doshi et al. teach that the payload is passed through the FEC decoder 255 (figure 2, col. 7, lines 12-13, Doshi et al.). Doshi et al. also teach that the exact number of decoders at the receiver may be one, as described herein with respect to sequential decoding or greater, if parallel decoding is desired (col. 17, lines 56-59, Doshi et al.). Doshi et al. teach that FEC is implemented by applying an algorithm to data to generate redundant bits at the transmitter (col. 1, lines 42-43, Doshi et al.). Doshi et al. also teach a forward error correction (FEC) encoder (item 215 in figure 2, col. 6, lines 61-62, Doshi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Doshi et al. by including additionally the encoder means further having means for generating and, in a sequence expected by said encoded symbol decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said encoder means input means; the encoder means being functionally interconnected to said

modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means; such that in use said encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof, in optional combination with at least one encoded reserved symbol in a pattern expected by said decoder means, said sequence of bits being caused to arrive at said decoding means; and said encoded symbol decoder means having error detection means such that in use said encoded symbol decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine and e. causing said encoded symbol decoder means to, if detecting a present unexpected or absent expected, encoded reserved symbol perform a selection from the group.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to transmit the encoded symbols to a receiver system with decoder in a separate location over the transmission system. The sequential decoding system and forward error correction is used at the receiver to detect and correct errors in the data received.

Sayood et al. also do not explicitly teach specifically that the sequential decoder means comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits. A selection from the group consisting of: at least one bistable element in said sequential decoding means is changed; and selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means; is performed and e. perform a selection from the group consisting of : change at least one bistable element in said sequential decoder means; and select a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means.

However Eerenstein et al. in an analogous art teach that the invention will be described in detail hereinafter with reference to the sequential finite-state machine whose state transition diagram is shown in FIG. 1. The FSM has 16 states and various transitions there between which are controlled by a clock

signal and an input signal. The input signal is in this case a bivalent type ("0" or "1"). Generally speaking, an input signal may also consist of more bits. At instants, which are defined by the clock signal, for example at to each position going edge, the finite-state machine changes over to a next state. The state bearing the number 1 is absorbing in the case of a sequence of 5 successive input signals having the value "1": the rest state 1 is reached from any rest state after at the most 5 ones of the input signal. The given sequence of X values of the input signal [c(0), c(1), . . . , c(X-1)] in this case appears as follows: ["1", "1", "1", "1", "1"]; X=5 and N=4. It will be apparent that these values have been chosen merely by way of example; other choices are also possible. This sequential finite-state machine can be implemented in a circuit by means of 4 bistable element flip-flops (2 to the power of 4 implies 16 feasible states), and a set of combinatory logic, which realizes the correct transitions between the states (figure 1, col. 3, lines 48-68, col. 4, lines 1-3, Eerenstein et al.).

Eerenstein et al. also teach that a sequential finite state machine circuit, comprising a set of N bistable elements [FF(1), . . . , FF(N)] and a set of combinatory logic connected thereto, the combination of logic values of the bistable elements defining a state of the circuit which is a representation of a state of a finite state machine, the circuit changing over to a next state at instants which are determined by a clock signal under the influence of the combinatory logic, the current state of the circuit, and an input signal, the set of combinatory logic realizing transitions between states of the finite-state machine in the circuit, characterized in that from any state a rest state is reached by way of a given sequence of X values of the input signal, [c(0), c(1), . . . , c(X-1)], starting with c(0) every sub-sequence [c(0), c(1), . . . , c(J-1)], having the length J, occurring in the given sequence of X values of the input signal, where 1<=J<=X, or a sub-sequence having the length J which is a one-to-one representation thereof being stored in the circuit.

The sequential finite-state machine circuit characterized in that the N bistable elements are presettable, the circuit being provided with (X-1) further bistable elements, coupled as a shift register, for the storage of the (X-1) most recent values of the input signal or values which are a one-to-one representation thereof, and is also provided with decoding logic, fed by the input signal and the (X-1) bistable elements of the shift register, which logic forms a detection signal as regards the occurrence of the given sequence

of X values of the input signal, said detection signal being applied as a preset signal to the N presettable bistable elements (col. 7, lines 30-59, col. 8, lines 1-2, Eerenstein et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Eerenstein et al. by including an additional step of using the sequential decoder means that comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits. A selection from the group consisting of: at least one bistable element in said sequential decoding means is changed; and selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means; is performed and e. perform a selection from the group consisting of: change at least one bistable element in said sequential decoder means; and select a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to perform error correction by the decoder, when an unexpected encoded symbol is received by the receiver.

Sayood et al. also do not explicitly teach specifically that

a. the decoding means comprises a functional combination of a sequential decoder means and an encoded symbol decoder means

d. causing said modulation-transmission means to enter said at least some of said plurality of encoded symbols into said functional combination of said sequential decoder means and encoded symbol decoder means.

However Agazzi in an analogous art teaches that the sequential decoder 58 looks at all signals from all four channels at the same time and at successive samples from each channel over several periods of unit time. A sequential decoder receives as input at least one signal from each of the first devices 56. The sequential decoder 58, in general, is responsive to the sequences of the output signals from the first

devices 56 for (1) passing acceptable sequences of such signals and (2) discarding unacceptable sequences of such signals in accordance with the constraints established by the code standard associated with the system (figure 6, col. 7, lines 57-66, Agazzi). Agazzi teaches that the second detector 60 is a symbol-by-symbol detector (figure 6, col. 8, lines 4-5, Agazzi).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Agazzi by including an additionally that a. the decoding means comprises a functional combination of a sequential decoder means and an encoded symbol decoder means, d. causing said modulation-transmission means to enter said at least some of said plurality of encoded symbols into said functional combination of said sequential decoder means and encoded symbol decoder means.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a functional combination of said sequential decoder means and encoded symbol decoder means would provide the opportunity to pass acceptable sequences of the signals and discard unacceptable sequences of the signals and detect errors in the signals received.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sayood et al. (Implementation issues in MAP joint source/channel coding, Proc. 22nd Annular Asilomar Conf. on Circuits, Systems, and Computers, pages 102-105, IEEE, November 1988) in view of Doshi et al. (US 6,349,138 B1), Eerenstein et al. (US 5,097,151), Kimura et al. (US 5,311,177) and Tajima (JP 63215226 A).

As per claim 17, Sayood et al. teach a method of correcting errors in decoded symbols which are encoded by an encoder in a joint source-channel coding system (page 102, Sayood et al.), comprises the steps of: a. providing a joint source-channel encoding (page 102, Sayood et al.), symbol decoding (page 104, Sayood et al.) and error correction system (page 102, Sayood et al.) comprising: an encoder means (pages 102-103, Sayood et al).; modulation-transmission means i.e. a channel (page 102, Sayood et al.); and decoding means (pages 102, 104, Sayood et al.). Sayood et al. teach the encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting

an encoded sequence of bits for allowed symbols input there into (page 102, Sayood et al.). Sayood et al. teach entering a sequence of symbols into the encoder means such that said sequence of symbols are encoded and exited therefrom as a binary bit stream sequence (page 102, Sayood et al.). Sayood et al. teach a branch and a path metric (pages 103-104, Sayood et al.). Sayood et al. teach detection of an error by the decoder means and monitoring output from the decoder means for errors (pages 102, 104, Sayood et al.).

However Sayood et al. do not explicitly teach specifically that the encoder means further having means for generating and, in a sequence expected by the decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to the encoder means input means; the encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means; such that in use the encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof in optional combination with at least one encoded reserved symbol in a pattern expected by the decoder means, said sequence of bits being caused to arrive at said arrive at said decoding means; and the decoder means having error detection means such that in use the decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine.

Doshi et al. in an analogous art teach that the output of the FEC encoder 215 is then prefixed with a framing byte at the framer 220, passed through a modulator 225 and broadcasted over the hybrid fiber/coax network 235 via a transmitter 230 for ultimate reception at individual cable modems 251 (figure 2, col. 7, lines 1-5, Doshi et al.). Doshi et al. teach that the payload is passed through the FEC decoder 255 (figure 2, col. 7, lines 12-13, Doshi et al.). Doshi et al. also teach that the exact number of decoders at the receiver may be one, as described herein with respect to sequential decoding or greater, if parallel decoding is desired (col. 17, lines 56-59, Doshi et al.). Doshi et al. teach that FEC is implemented by applying an algorithm to data to generate redundant bits at the transmitter (col. 1, lines 42-43, Doshi et

al.). Doshi et al. also teach a forward error correction (FEC) encoder (item 215 in figure 2, col. 6, lines 61-62, Doshi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Doshi et al. by including an additional step of using the encoder means further having means for generating and, in a sequence expected by the decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to the encoder means input means; the encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means; such that in use the encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof in optional combination with at least one encoded reserved symbol in a pattern expected by the decoder means, said sequence of bits being caused to arrive at said arrive at said decoding means; and the decoder means having error detection means such that in use the decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to transmit the encoded symbols over the transmission system to a receiver system with decoder in a separate location. The sequential decoding system and forward error correction is used at the receiver to detect and correct errors in the data received.

Sayood et al. also do not explicitly teach the specific use of the system, which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, specific bistable elements in said sequential decoder means being identified as fixed branch points and a selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means at said specified branch points; is performed; d. producing a plurality of series of sequential bits which

result from the changing of bistable elements in said sequential decoder means at said branch points by using fixed branch point bistable elements in said sequential decoder means; e. determining which series of sequential bits in said produced plurality of series of sequential bits is most likely correct.

However Eerenstein et al. in an analogous art teach that the invention will be described in detail hereinafter with reference to the sequential finite-state machine whose state transition diagram is shown in FIG. 1. The FSM has 16 states and various transitions there between which are controlled by a clock signal and an input signal. The input signal is in this case a bivalent type ("0" or "1"). Generally speaking, an input signal may also consist of more bits. At instants, which are defined by the clock signal, for example at to each position going edge, the finite-state machine changes over to a next state. The state bearing the number 1 is absorbing in the case of a sequence of 5 successive input signals having the value "1": the rest state 1 is reached from any rest state after at the most 5 ones of the input signal. The given sequence of X values of the input signal [c(0), c(1), . . . , c(X-1)] in this case appears as follows: ["1", "1", "1", "1", "1"]; X=5 and N=4. It will be apparent that these values have been chosen merely by way of example; other choices are also possible. This sequential finite-state machine can be implemented in a circuit by means of 4 bistable element flip-flops (2 to the power of 4 implies 16 feasible states), and a set of combinatory logic, which realizes the correct transitions between the states (figure 1, col. 3, lines 48-68, col. 4, lines 1-3, Eerenstein et al.).

Eerenstein et al. also teach that a sequential finite state machine circuit, comprising a set of N bistable elements [FF(1), . . . , FF(N)] and a set of combinatory logic connected thereto, the combination of logic values of the bistable elements defining a state of the circuit which is a representation of a state of a finite state machine, the circuit changing over to a next state at instants which are determined by a clock signal under the influence of the combinatory logic, the current state of the circuit, and an input signal, the set of combinatory logic realizing transitions between states of the finite-state machine in the circuit, characterized in that from any state a rest state is reached by way of a given sequence of X values of the input signal, [c(0), c(1), . . . , c(X-1)], starting with c(0) every sub-sequence [c(0), c(1), . . . , c(J-1)], having the length J, occurring in the given sequence of X values of the input signal, where 1<=J<=X,

or a sub-sequence having the length J which is a one-to-one representation thereof being stored in the circuit.

The sequential finite-state machine circuit characterized in that the N bistable elements are presettable, the circuit being provided with (X-1) further bistable elements, coupled as a shift register, for the storage of the (X-1) most recent values of the input signal or values which are a one-to-one representation thereof, and is also provided with decoding logic, fed by the input signal and the (X-1) bistable elements of the shift register, which logic forms a detection signal as regards the occurrence of the given sequence of X values of the input signal, said detection signal being applied as a preset signal to the N presettable bistable elements (col. 7, lines 30-59, col. 8, lines 1-2, Eerenstein et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Eerenstein et al. by including an additional step of using the system, which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, specific bistable elements in said sequential decoder means being identified as fixed branch points and a selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means at said specified branch points; is performed; d. producing a plurality of series of sequential bits which result from the changing of bistable elements in said sequential decoder means at said branch points by using fixed branch point bistable elements in said sequential decoder means; e. determining which series of sequential bits in said produced plurality of series of sequential bits is most likely correct.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to perform error correction by the decoder when an unexpected encoded symbol is received by the receiver.

Sayood et al. also do not explicitly teach specifically that the encoder means is an arithmetic encoder and the decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder.

However Kimura et al. in an analogous art teach that FIG. 4 is a block diagram of the structure of a code transmitting apparatus in this embodiment. An arithmetic encoder 302 of a one-time 2-bits insertion system generates an arithmetic code 315. An arithmetic decoder 303 of a one-time 2-bits insertion system detects and processes the carry control signal by using the arithmetic code 315 supplied from the arithmetic encoder 302 (figure 4, col. 21, lines 17-19, lines 27-29, lines 40-43, Kimura et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Kimura et al. by including additionally that the encoder means is an arithmetic encoder and the decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using an arithmetic encoder and an arithmetic decoder would provide the opportunity to use data compressing/expanding method for high performance transmission with error detection.

Sayood et al. also do not explicitly teach specifically that the decoding means comprises a functional combination of a sequential decoder means and an arithmetic decoder means.

However Tajima in an analogous art teaches that to reduce the number of processing steps, and to improve the processing speed by constituting the titled (i.e. sequential) decoder of a syndrome forming device, a buffer memory inputting and preserving a syndrome series and preserving and outputting an error series, a sequential decoding arithmetic circuit, and a correcting circuit correcting a data corresponding to an information symbol in a received data. A sequential decoding arithmetic circuit has a state trellis corresponding to the syndrome forming device in its inside to transit the state of trellis based on the syndrome series fetched from a buffer memory (abstract, Tajima).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sayood et al.'s patent with the teachings of Tajima by including additionally that the decoding system comprises a functional combination of a sequential decoder system and an arithmetic decoder system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding means comprising a functional combination of a sequential decoder means and an arithmetic decoder means would provide the opportunity to pass acceptable sequences of the signals and discard unacceptable sequences of the signals and to use data compressing/expanding method for high performance transmission with error detection.

Allowable Subject Matter

9. Claims 12-16 are allowed.

The following is an examiner's statement of reasons for allowance:

As per the claim 12, Sayood et al. (Implementation issues in MAP joint source/channel coding, Proc. 22nd Annular Asilomar Conf. on Circuits, Systems, and Computers, pages 102-105, IEEE, November 1988) teach a method of correcting errors in decoded symbols which are encoded by an encoder in a joint source-channel coding system (page 102, Sayood et al.), comprises the steps of: a. providing a joint source-channel encoding (page 102, Sayood et al.), symbol decoding (page 104, Sayood et al.) and error correction system (page 102, Sayood et al.) comprising: an encoder means (pages 102-103, Sayood et al.); modulation-transmission means i.e. a channel (page 102, Sayood et al.); and decoding means (pages 102, 104, Sayood et al.). Sayood et al. teach that the encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input there into (page 102, Sayood et al.).

Doshi et al. (US 6,349,138 B1) teach a sequential decoder means (col. 17, lines 56-59, Doshi et al.). Doshi et al. teach said the encoder means further having means for generating and, in a sequence expected by said the decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to the encoder means input means (FEC encoder 215 in figure 2, col. 1, lines 42-43, col. 6, lines 61-62, Doshi et al.). Doshi et al. teach that the encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means (figure 2, col. 7, lines 1-5, lines 12-13, Doshi et al.).

Doshi et al. teach that the encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof in optional combination with at least one encoded reserved symbol in a pattern expected by the decoder means, the sequence of bits being caused to arrive at said decoding means (col. 1, lines 38-46, Doshi et al.); and the decoder means having error detection means such that in use the decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine (col. 2, lines 64-67, Doshi et al.).

Eerenstein et al. (US 5,097,151) teach a system, which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits and at least one bistable element in said sequential decoder means is changed (figure 1, col. 3, lines 48-68, col. 4, lines 1-3, Eerenstein et al.).

Kimura et al. (US 5,311,177) teach that the encoder means is an arithmetic encoder and the decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder (figure 4, col. 21, lines 17-19, lines 27-29, lines 40-43, Kimura et al.).

Tajima (JP 63215226 A) teaches that the decoding means comprises a functional combination of a sequential decoder means and an arithmetic decoder means (abstract, Tajima).

However Sayood et al., Doshi et al., Eerenstein et al., Kimura et al. and Tajima do not teach specifically

b. entering a sequence of symbols into said arithmetic encoder such that said sequence of symbols are encoded and exited therefrom as a binary bit stream sequence of +x $\sqrt{Es}$ and -x $\sqrt{Es}$ signals, corresponding to a string of "1"/("0")'s and "0"/("1")'s which pass through said transmission channel and enter said sequential decoder means, where x is a fraction;

c. making hard logic circuitry decisions as to the presence of "1"/("0")'s and "0"/("1")'s based on said binary bit stream sequence of + x $\sqrt{Es}$ and - x $\sqrt{Es}$ signals while identify decisions based upon signals wherein x is of a value so as to cause the values of + x $\sqrt{Es}$ or - x $\sqrt{Es}$ to be within a null zone of + DELTA to -DELTA around 0.0, and identifying said decisions as "branch point" decisions in said sequential decoder means;

d. monitoring output from said arithmetic decoder for errors and when an error is indicated thereby, identifying a "branch point" in said sequential decoder means and correcting the "1"/("0") or "0"/("1") based binary bit thereat by inverting it to "0"/("1") or "1"/("0").

For these reasons, claim 12 is allowed. Claims 13-16 are allowed because of the combination of additional limitations and the limitations listed above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

10. Claim 18 is objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

The present invention pertains to a method of correcting errors in decoded symbols, which are encoded by an arithmetic encoder in a joint source-channel coding system. As per claim 18, Tajima (JP 63215226 A) teaches that the decoding means comprises a functional combination of a sequential decoder means and an arithmetic decoder means (abstract, Tajima). Sayood et al. (Implementation issues in MAP joint source/channel coding, Proc. 22nd Annular Asilomar Conf. on Circuits, Systems, and Computers, pages 102-105, IEEE, November 1988) teach an error correction system (page 102, Sayood et al.). However the prior art of record do not teach determination of which series of sequential bits in the produced plurality of series of sequential bits is most likely correct, involves at least one selection from the group consisting of: a. eliminating any series of sequential bits which contains an encoded reserved symbol; b. applying a metric to at least two series of sequential bits which do not contain an encoded reserved symbol, to determine which of the at least two series of sequential bits is most likely correct; c. applying an Euclidean metric to at least two series of sequential bits which do not contain an encoded reserved symbol, to determine which of the at least two series of sequential bits is most likely correct. Hence the prior art taken alone or in any combination fail to teach the claimed novel feature in claim 18 in view of its base and intervening claims.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

Albert DeCady
Primary Examiner